

Form PTO 1449  U.S. Department of Commerce Patent and Trademark Office  Information Disclosure Statement by Applicant	ATTY. DOCKET NUMBER NITT.0155	SERIAL NUMBER 10/660,657
	APPLICANT Hanzawa et al	
	FILING DATE 09/12/03	GROUP AV 2824

**U.S. Patent Documents**

Examiner Initial	Cited in parent	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
at	X	4,408,304	10/4/83	Nishizawa et al	365	174	5/4/81
at	X	6,314,017 B1	11/6/2001	Emori et al	365	149	7/21/2000
at	X	6,512,714 B2	1/28/2003	Hanzawa et al.	365	210	8/31/2001

**Foreign Patent Documents**

Examiner Initial	Cited in parent	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
							YES	NO
at	X	9-213812	08/1997	Japan	H01L	21/8242	Abstract	X

**Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)**

at	Cited in parent	Regitz, W. M., "A Three-Transistorcell, 1024-Bit, 500 NS MOS RAM," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 1970, pp. 42-43
at	Cited in parent	Nakazato, Kazuo et al., "Phase-state Low Electron-number Drive Random Access Memory (PLEDM)," IEEE International Solid-State Circuits Conferences, Digest of Technical Papers, 2000, pp. 132-133

EXAMINER 	DATE CONSIDERED 02/19/2004
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*EXAMINER: Initial if citation is considered, whether or not citation is in conformance with MPEP 609; draw a line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant*